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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/751,674	12/29/2000	Paolo Faraboschi	00-BN-059 (STMI01-00059)	9124

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EXAMINER	
LI, AIMEE J	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 04/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/751,674	FARABOSCHI ET AL.	
	Examiner	Art Unit	
	Aimee J Li	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 January 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-22 have been considered.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: RCE as received on 19 January 2005 and Amendment as received on 19 January 2005.

Specification

3. The disclosure is objected to because of the following informalities:

4. Please revise the Summary of Invention. The current Summary of Invention is merely a repeat of the claims. This does not "set out the exact nature, operation, and purpose" nor provide "material assistance in aiding ready understanding of the patent in future searches of the invention" as set forth in MPEP § 608.01(d).

5. Appropriate correction is required.

Claim Rejections - 35 USC § 112

6. Claim 20 is objected to because of the following informalities: Claim 20 recites "wherein L=4 and C" when the original claim recites "wherein L=4 and C=3". The Examiner believes it is a typographical error on the part of the Applicant and requests that this error be corrected. Appropriate correction is required.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. Claims 1-3, 8-12, and 17-22 are rejected under 35 U.S.C. 102(e) as being taught by Jouppi, U.S. Patent Number 6,167,503 (herein referred to as Jouppi).

9. Referring to claims 1, 10, 21, and 22, Jouppi has taught a processing system comprising:

a. A data processor (Applicant's claim 10) (Jouppi column 2, lines 61-64 and Figure 1);

b. A memory coupled to said data process (Applicant's claim 10) (Jouppi column 3, liens 16-25 and Figure 1);

c. A plurality of memory-mapped peripheral circuits coupled to said data processor for performing selected functions in association with said data processor (Applicant's claim 10) (Jouppi column 3, lines 16-65 and Figure 1);

d. Wherein said data processor comprises:

i. C execution clusters (Applicant's claims 1 and 10) (Jouppi Abstract, lines 8-9; column 2, lines 22-30; column 4, lines 25-38; Figure 2A; and Figure 2B), each of said C execution clusters comprising

(1) An instruction execution pipeline having N processing stages capable of executing instruction bundles comprising from one to S syllables (Applicant's claims 1 and 10) (Jouppi Abstract, lines 8-9; column 2, lines 22-30; column 4, lines 25-38; Figure 2A; and Figure 2B). In regards to Jouppi, a superscalar processor like Jouppi's is inherently a pipelined processor. A superscalar

processor is a basic pipelined processor that is expanded to execute more than one pipeline at once. Please see Vasilevsky et al., U.S. Patent Number 5,274,818 (column 2, line 67 to column 3, line 7); "Pipelining", and Chien's "Superscalar Execution" for more information on pipelining and superscalar processors.

(2) Wherein each of said instruction execution pipelines is L lanes wide (Applicant's claims 1 and 10) (Jouppi column 4, lines 25-32; column 5, lines 41-52; column 6, lines 8-14; Figure 2A; and Figure 2B). In regards to Jouppi, the Applicant's specification has not explicit definition that the Examiner could locate for the term "Lane". When referring to Applicant's Figure 5 and Figure 8 and their respective descriptions in the specification, "Lane" seems to refer to the specific execution units within the clusters receiving the syllables. Then, the "Lanes" in *Jouppi* would be the specific execution units 250 and 251 in the execution clusters 280 and 290 in *Jouppi*'s Figures 2A and 2B.

(3) Each of said L lanes capable of receiving one of said one to S syllables of said instruction bundles (Applicant's claims 1 and 10) (Jouppi column 4, lines 25-32; column 5, lines 41-52; column 6, lines 8-14; Figure 2A; and Figure 2B).

ii. Aligning said syllables with correct ones of said lanes (Applicant's claims 21 and 22).An instruction cache capable of storing a plurality of cache

lines, each of said cache lines comprising C*L syllables (Applicant's claims 1 and 10) (Jouppi column 3, lines 58-65; column 4, lines 9-19; Figure 2A; and Figure 2B);

iii. An instruction issue unit capable of receiving fetched ones of said plurality of cache lines and issuing complete instruction bundles toward said C execution clusters (Applicant's claims 1 and 10) (Jouppi column 4, lines 25-38; Figure 2A; and Figure 2B); and

iv. Alignment and dispersal circuitry capable of receiving said complete instruction bundles from said instruction issue unit and routing each of said received complete instruction bundles to a correct one of said C execution clusters as a function of at least one address bit associated with each of said complete instruction bundles (Applicant's claims 1, 10, 21, and 22) (Jouppi column 2, lines 9-13; column 4, lines 25-38; column 7, lines 6-30; column 8, lines 11-36; Figure 2A; and Figure 2B).

10. Referring to claims 2 and 11, Jouppi has taught wherein said alignment and dispersal circuitry routes each of said received complete instruction bundles to said correct execution cluster as a function of at least one address bit associated with at least one syllable in each of said complete instruction bundles (Jouppi column 2, lines 9-13; column 4, lines 25-38; column 7, lines 6-30; column 8, lines 11-36; Figure 2A; and Figure 2B).

11. Referring to claims 3 and 12, Jouppi has taught wherein said alignment and dispersal circuitry routes each of said received complete instruction bundles to said correct execution

cluster as a function of a cluster bit associated with each of said complete instruction bundles (Jouppi column 4, lines 53-63; Figure 2A; and Figure 2B).

12. Referring to claims 8 and 17, Jouppi has taught wherein L=4 (Jouppi column 4, lines 25-32; column 5, lines 41-52; column 6, lines 8-14; Figure 2A; and Figure 2B). In regards to Jouppi, the execution units 250 and 251 show four individual ones.

13. Referring to claims 9 and 18, Jouppi has taught wherein C=3 (Jouppi column 5, lines 41-42 and column 10, lines 32-42).

14. Referring to claim 19, Jouppi has taught for use in a data processor C execution clusters (Jouppi Abstract, lines 8-9; column 2, lines 22-30; column 4, lines 25-38; Figure 2A; and Figure 2B), each of said C execution clusters comprising

a. An instruction execution pipeline having N processing stages capable of executing instruction bundles comprising from one to S syllables (Applicant's claims 1 and 10) (Jouppi Abstract, lines 8-9; column 2, lines 22-30; column 4, lines 25-38; Figure 2A; and Figure 2B). In regards to Jouppi, a superscalar processor like Jouppi's is inherently a pipelined processor. A superscalar processor is a basic pipelined processor that is expanded to execute more than one pipeline at once. Please see Vasilevsky et al., U.S. Patent Number 5,274,818 (column 2, line 67 to column 3, line 7); "Pipelining", and Chien's "Superscalar Execution" for more information on pipelining and superscalar processors.

b. Wherein each of said instruction execution pipelines is L lanes wide (Applicant's claims 1 and 10) (Jouppi column 4, lines 25-32; column 5, lines 41-52; column 6, lines 8-14; Figure 2A; and Figure 2B). In regards to Jouppi, the Applicant's

specification has not explicit definition that the Examiner could locate for the term "Lane". When referring to Applicant's Figure 5 and Figure 8 and their respective descriptions in the specification, "Lane" seems to refer to the specific execution units within the clusters receiving the syllables. Then, the "Lanes" in *Jouppi* would be the specific execution units 250 and 251 in the execution clusters 280 and 290 in *Jouppi*'s Figures 2A and 2B.

c. Each of said L lanes capable of receiving one of said one to S syllables of said instruction bundles (Applicant's claims 1 and 10) (Jouppi column 4, lines 25-32; column 5, lines 41-52; column 6, lines 8-14; Figure 2A; and Figure 2B).

d. A method of routing instruction bundles into the L lanes in the C execution clusters comprising the steps of:

i. Fetching cache lines from an instruction cache, each of said cache lines comprising C*L syllables (Jouppi column 3, lines 58-65; column 4, lines 9-19; Figure 2A; and Figure 2B);

ii. Issuing complete instruction bundles toward the C execution clusters (Jouppi column 4, lines 25-38; Figure 2A; and Figure 2B); and

iii. Routing each of the received complete instruction bundles to a correct one of the C execution clusters as a function of at least one of (Jouppi column 2, lines 9-13; column 4, lines 25-38; column 7, lines 6-30; column 8, lines 11-36; Figure 2A; and Figure 2B):

(1) At least one address bit associated with each of the complete instruction bundles (Jouppi column 2, lines 9-13; column 4, lines

25-38 and 53-63; column 7, lines 6-30; column 8, lines 11-36; Figure 2A; and Figure 2B);

(2) At least one address bit associated with at least one syllable in each of the complete instruction bundles (Jouppi column 2, lines 9-13; column 4, lines 25-38 and 53-63; column 7, lines 6-30; column 8, lines 11-36; Figure 2A; and Figure 2B); and

(3) A cluster bit associated with each of the complete instruction bundles (Jouppi column 2, lines 9-13; column 4, lines 25-38 and 53-63; column 7, lines 6-30; column 8, lines 11-36; Figure 2A; and Figure 2B).

15. Referring to claim 20, Jouppi has taught wherein L=4 (Jouppi column 4, lines 25-32; column 5, lines 41-52; column 6, lines 8-14; Figure 2A; and Figure 2B) and C=3 (Jouppi column 5, lines 41-42 and column 10, lines 32-42). In regards to Jouppi, the execution units 250 and 251 show four individual ones.

Claim Rejections - 35 USC § 103

16. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

17. Claims 4-7 and 13-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jouppi, as applied to claims 1 and 10 above, and further in view of Sachs et al., U.S. Patent

Number 5,560,028 (herein referred to as Sachs). Jouppi has taught wherein said control logic circuitry controls said multiplexer circuitry as a function of at least one of:

a. Said at least one address bit associated with each of said complete instruction bundles (Applicant's claims 7 and 16) (Jouppi column 2, lines 9-13; column 4, lines 25-38 and 53-63; column 7, lines 6-30; column 8, lines 11-36; Figure 2A; and Figure 2B);

b. At least one address bit associated with at least one syllable in each of said complete instruction bundles (Applicant's claims 7 and 16) (Jouppi column 2, lines 9-13; column 4, lines 25-38 and 53-63; column 7, lines 6-30; column 8, lines 11-36; Figure 2A; and Figure 2B); and

c. A cluster bit associated with each of said complete instruction bundles (Applicant's claims 7 and 16) (Jouppi column 2, lines 9-13; column 4, lines 25-38 and 53-63; column 7, lines 6-30; column 8, lines 11-36; Figure 2A; and Figure 2B).

18. Jouppi has not taught

a. Wherein said alignment and dispersal circuitry routes each of said received complete instruction bundles to said correct execution cluster as a function of a stop bit associated with at least one syllable in each of said complete instruction bundle (Applicant's claims 4 and 13);

b. Wherein said alignment and dispersal circuitry comprises multiplexer circuitry capable of routing each of said received complete instruction bundle to any one of said C execution clusters (Applicant's claims 5 and 14); and

c. Wherein said alignment and dispersal circuitry comprises control logic circuitry capable of controlling said multiplexer circuitry (Applicant's claims 6 and 15).

19. However, Jouppi has taught instruction dispersal circuitry (Jouppi column 2, lines 9-13; column 4, lines 25-38; column 7, lines 6-30; column 8, lines 11-36; Figure 2A; and Figure 2B). Sachs has taught instruction dispersal circuitry

a. Wherein said alignment and dispersal circuitry routes each of said received complete instruction bundles to said correct execution cluster as a function of a stop bit associated with at least one syllable in each of said complete instruction bundles (Applicant's claim 4) (Sachs column 3, lines 11-18; column 9, lines 3-6 and 30-62; Figure 8; and Figure 10);

b. Wherein said alignment and dispersal circuitry comprises multiplexer circuitry capable of routing each of said received complete instruction bundles to any one of said C execution clusters (Applicant's claim 5) (Sachs column 3, lines 11-18; column 9, lines 3-6 and 30-62; Figure 8; and Figure 10); and

c. Wherein said alignment and dispersal circuitry comprises control logic circuitry capable of controlling said multiplexer circuitry (Applicant's claim 6) (Sachs column 3, lines 11-18; column 9, lines 3-6 and 30-62; Figure 8; and Figure 10).

20. A person of ordinary skill in the art at the time the invention was made would have recognized that the instruction dispersal circuitry ensures the correct execution cluster executes the instruction bundles, thereby ensuring valid and correct data. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the dispersal circuitry of Sachs in the device of Jouppi to ensure valid and correct data.

Response to Arguments

21. Examiner withdraws the specification objection to the Abstract in favor of the amended Abstract.

22. Applicant argues in essence on page 13

> ...Office Action fails to provide any explanation as to why the Summary in this particular application does not 'set out the exact nature, operation, and purpose' of the invention or provide 'material assistance in aiding ready understanding of the patent.'

23. This has not been found persuasive. Applicant's "Summary of the Invention" on pages 12-13 do not aid in understanding of the patent. The majority of the summary language is exactly the same as the claim language, which required numerous readings to fully comprehend what is being claimed. The amendments made to the Abstract clearly state the exact nature of the apparatus described in Applicant's specification without requiring numerous readings to understand, especially regarding the exact inter-dependencies of some of the elements. For example, the amended Abstract states "Each execution cluster includes an instruction execution pipeline having a number of processing stages, and each execution pipeline is a number of lanes wide. The processing stages execute instruction bundles, where each instruction bundle has one or more syllables. Each lane is capable of receiving one of the syllables of an instruction bundle." This is easier to understand upon an initial reading than "...each of the C execution clusters comprising an instruction execution pipeline having N processing stages capable of executing instruction bundles comprising from one to S syllables, wherein each the instruction execution pipelines is L lanes wide, each of the L lanes capable of receiving one of the one to S

syllables of the instructions bundles;...". The language used in the claims, while appropriate for claims, are not necessarily appropriate for the summary, since the summary is supposed to aid in "ready understanding of the patent."

24. Applicant argues in essence on page 16

> ...Office Action fails to show that *Jouppi* discloses, teaches, or suggests an "instruction cache" capable of storing cache lines, each of the cache lines including "C*L syllables" (where C=number of execution clusters and L=number of lanes)...Nothing in the cited portions of *Jouppi* recite that each cache line includes "C*L syllables" (where C=number of execution clusters and L=number of lanes)...

25. This has not been found persuasive. The Applicant's specification has no explicit definition that the Examiner could locate for the term "Lane". When referring to Figure 5 and Figure 8 and their respective descriptions in the specification, "Lane" seems to refer to the specific execution units within the clusters receiving the syllables. Then, the "Lanes" in *Jouppi* would be the specific execution units 250 and 251 in the execution clusters 280 and 290 in *Jouppi*'s Figures 2A and 2B. "Lanes" seems to refer to the individual execution units in the clusters. *Jouppi* has taught that the instructions are concurrently fetched from the cache, as can be seen in *Jouppi's* Figure 2A by the eight connections between the I-Cache and IDU. This means that each individual instruction, e.g. syllable from Applicant's specification, must be fetched from the same cache line being accessed at that point in time. In *Jouppi,* there are eight instructions fetched concurrently, which makes the C*L requirement. *Jouppi* has two clusters and each cluster has four lanes. This means that there must be eight syllables coming from the I-

Cache, which there are in *Jouppi*. As is explained in *Jouppi*, column 5, line 41 to column 6, line 14, each syllable is executed in the appropriate individual execution unit in one of the clusters.

Conclusion

26. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J Li whose telephone number is (571) 272-4169. The examiner can normally be reached on M-T 7:30am-5:00pm.

27. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

28. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AJL
Aimee J. Li
4 April 2005

RICHARD L. ELLIS
PRIMARY EXAMINER